Amendments To the Abstract of the Disclosure
(Marked-up Version)

The following is a marked-up version of the Abstract of the Disclosure to aid the Examiner in identifying the changes:

A data input device of a DDR SDRAM includes at least a clock pulse generator (for ~~receiving~~ outputting a data-in-strobe signal based on an internal clock), ~~which operates in a write mode, and outputting a data-in-strobe signal that is a first control signal, a~~ first and second data buffers (being ~~an operation of which is~~ controlled by the data-in-strobe signal and having ~~an~~ output lines ~~of which corresponds to a~~ corresponding to first and second global input-output lines, respectively). ~~of the DDR SDRAM, and a second data buffer an operation of which is controlled by the data-in-strobe signal and an output line of which corresponds to a second global input/output line of the DDR SDRAM. If~~ When a second control signal is ~~in a~~ low ~~level~~, the first data is directly applied to the first data buffer for ~~to be~~ transfer~~red~~ to the first global input-output line, and the second data is directly applied to the second data buffer ~~to be~~ for transfer~~red~~ to the second global input-output line. ~~If~~ When the second control signal is ~~in a~~ high ~~level~~, the first data is directly applied to the second data buffer ~~to be~~ for transfer~~red~~ to the second global input/-output line, and the second data is directly applied to the first data buffer ~~to be~~ for transfer~~red~~ to the first global input/-output line. The ~~data input device can reduce the~~ time for the write

operation is reduced by directly applying the write-in-strobe signal~~, which is enabled in the write mode,~~ to the data buffers~~, and it can also reduce the layout area~~.